REMARKS

Claim 9 has been amended. No claims have been canceled. Claims 10-25 are newly added. Accordingly, after entry of this Amendment, claims 1-25 will remain pending.

In the Office Action, the Examiner rejected claims 1-6 and 8 under 35 U.S.C. § 102(e) as anticipated by Hussey, Jr. et al. (U.S. Patent No. 6,728,591). Claims 7 and 9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Hussey, Jr. et al. in view of Reiss et al. (U.S. Patent Application Publication No. 2003/0014145). The Applicant respectfully disagrees with the rejections and, therefore, respectfully traverses the same.

Claims 1-6 and 8 are patentably distinguishable over Hussey, Jr. et al. because the claims recite a method of operating a semiconductor processing system that combines a number of features including, among them, determining first and second states for a wafer via optical digital profiling. Contrary to the Examiner's assertion, Hussey, Jr. et al. does not describe determining either first or second states via optical digital profiling. Specifically, Hussey, Jr. et al. describes a metrology tool 550 that acquires metrology data via "an optical measurement unit, such as a scatterometer." (Hussey, Jr. et al. at col. 7, lines 12-14.) As would be appreciated by those skilled in the art, a scatterometer is not an optical digital profiling tool since an optical digital profiling tool processes the optical data in a way that differs from a scatterometer. As a result, the Applicant respectfully submits that Hussey, Jr. et al. does not describe each and every feature as recited by claims 1-6 and 8 and, as a result, cannot anticipate those claims.

In addition, the Applicant respectfully submits that claim 7, which depends from claim 1, is patentably distinguishable over the combination of Hussey, Jr. et al. and Reiss et al.

Reiss et al. describes an integration of fault detection with run-to-run control. As previously recognized by the Examiner, Reiss et al. does not teach that the first and second states are determined via optical digital profiling. Moreover, the method described by Reiss

et al. differs from that recited by claim 7. Accordingly, the Applicant respectfully submits that Reiss et al. cannot be combined with Hussey, Jr. et al. to render obvious claim 7.

As recited by claim 7, the method includes, among other features, determining a process recipe to change the state of the wafer from the first state to the second state, performing the process recipe on the wafer, wherein the state of the wafer changes from the first state to a processed state, determining when the processed state is not the second state, and updating the process recipe, wherein the determining of the process recipe includes predicting the second state using the first state of the wafer and a process model based on the process conditions. In contrast, in Reiss et al. a predicted output is determined and compared with specification limits. If the predicted output is outside of the specification limits but within the tool range limits, the tool recipe may be modified. (Reiss et al. at paragraphs [0047] – [0049].) There is, among other things, no discussion of determining a second state for the wafer via optical digital profiling using critical dimension data and sidewall angle data. In addition, there is no discussion of determining when the processed state is not the second state and updating the process recipe. As a result, Reiss et al. cannot be combined properly with Hussey et al. to render claim 7 obvious.

The Applicant respectfully submits that claim 9 also cannot be rendered obvious for similar reasons that claim 7 cannot be rendered obvious. In addition, claim 9 has been modified so that several of the steps are performed substantially simultaneously. Support for this amendment may be found, for example, in paragraphs [0050], [0073], and [0080]. The references do not describe or suggest this additional feature. Accordingly, at least for this addition reason, claim 9 is patentable over the references relied upon by the Examiner.

Newly-added claims 10-17 follow the recitations of claims 1-8 except that determining the first and second states uses filtered metrology data. Support for these claims may be found at, for example, paragraphs [0074] though [0076]. In combination with the

other features recited by claims 10-17, this additional feature is not disclosed or suggested by either Hussey, Jr. et al. or Reiss et al. Accordingly, the Applicant respectfully submits that claims 10-17 are patentable thereover.

Newly-added claims 18-25 follows the recitation of claims 1-8 except that determining the first and second states comprises measuring a bottom critical dimension in a gate stack. Support for these claims may be found, for example, at paragraph [0012]. In combination with the other features recited by claims 18-25, this additional feature also is not described or suggested by Hussey, Jr. et al. or Reiss et al. Accordingly, the Applicant respectfully submits that claims 18-25 are patentable thereover.

Each of the rejections having been addressed, the Applicant respectfully submits that the claims are now in condition for allowance and a notice to that effect is respectfully requested.

If there are any fees due in connection with the filing of this paper that are not otherwise accounted for, please charge our Deposit Account No. 03-3975 and refer to Order No. 071469/0304316.

Respectfully submitted,

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